What is claimed is:

1. An imager comprising:

an array comprised of imager cells; and

a multi-mode controller coupled to the array, the multi-mode controller comprising circuitry implementing at least one of a high-light mode of operation providing charge accumulation in a photoreceptor potential well and a readout potential well, and a Snap mode of operation simultaneously transferring accumulated charge for a set of the imager cells to their sense nodes.

2. The imager of claim 1, wherein the high-light mode provides charge accumulation in the photoreceptor potential well, the readout potential well, and a sense node potential well.

3. The imager of claim 1, wherein the high-light mode comprises a V+ integration voltage applied during an integration period to a photoreceptor readout gate, thereby allowing charge to accumulate in the readout potential well.

4. The imager of claim 3, wherein the V+ integration voltage comprises one of a plurality of V+ integration voltages available to the multi-mode controller for setting up a selected charge capacity in one of the imager cells.

5. The imager of claim 1, wherein the multi-mode controller further comprises circuitry for implementing a low-light mode providing charge accumulation in the photoreceptor potential well and constrained by an integration potential well during an integration period.

6. The imager of claim 1, wherein at least one of the imager cells comprises a pinned photoreceptor.

7. The imager of claim 1, wherein at least one of the imager cells comprises a pinned photodiode.

8. The image of claim 1, wherein at least one of the imager cells comprises an anti-reflective coating.

9. An imager comprising:

an array comprised of imager cells; and

a multi-mode controller coupled to the array, the multi-mode controller comprising circuitry implementing a high-light mode of operation providing charge accumulation in a photoreceptor potential well and a readout potential well, and a low-light mode operation providing charge accumulation in the photoreceptor potential well and constrained by an integration potential well.

10. The imager of claim 9, wherein the high-light mode of operation provides charge accumulation in the photoreceptor potential well, the readout potential well, and a sense node potential well.

11. The imager of claim 9, wherein the multi-mode controller determines to use the high-light mode or the low-light mode based on operator input.

12. The imager of claim 9, wherein the multi-mode controller determines to use the high-light mode or the low-light mode based upon light sensor input.

13. The imager of claim 9, wherein the high-light mode is characterized by a V+ integration voltage selected from one of a plurality of V+ integration voltages available

to the multi-mode controller for setting up a selected charge capacity in one of the imager cells.

14. The imager of claim 9, wherein the multi-mode controller further comprises circuitry implementing a Snap mode of operation simultaneously transferring accumulated charge for a set of the imager cells to their sense nodes.

15. An imager comprising:

means for accumulating electrons generated by photons incident on the imager; and

means for controlling the imager in accordance with multiple modes of operation comprising at least a high-light mode and a low-light mode.

16. The imager of claim 15, wherein the means for controlling the imager in the high-light mode comprises means for accumulating charge in a photoreceptor potential well and a readout potential well.

17. The imager of claim 16, wherein the means for controlling the imager in the high-light mode comprises means for accumulating charge in the photoreceptor potential well, the readout potential well, and a sense node potential well.

18. The imager of claim 15, wherein the means for controlling the imager in the low-light mode comprises means for accumulating charge in the photoreceptor potential well and constrained by an integration potential well.

19. The imager of claim 15, wherein the means for controlling comprises means for controlling the imager in accordance with a high-light mode, a low-light mode, and a Snap mode.

20. The imager of claim 19, wherein the means for controlling the imager in the Snap mode comprises means for simultaneously transferring accumulated charge from the means for accumulating electrons to sense nodes.

21. The imager of claim 19, wherein the means for controlling the imager further comprises means for setting up a selected charge capacity during high-light mode.

21. In an imager comprising an array of imager cells coupled to a multi-mode controller, a method for controlling the imager, the method comprising:

selecting between a low-light operating mode and a high-light operating mode;

when operating in the high-light operating mode, collecting electrons in a photoreceptor potential well and a readout potential well; and

when operating in the low-light operating mode, collecting electrons in the photoreceptor potential well and constrained by an integration potential well.

22. The method of claim 21, further comprising, when operating in the high-light operating mode, collecting electrons in a sense node potential well.

23. The method of claim 21, further comprising, when operating in the high-light operating mode, establishing a V+ integration voltage on a photoreceptor readout gate.

24. The method of claim 23, wherein establishing further comprises establishing a V+ integration voltage selected from one of a plurality of V+ integration voltages available to the multi-mode controller for setting up a selected charge capacity in one of the imager cells.

25. The method of claim 21, further comprising, when operating in the low-light operating mode, establishing a V- integration voltage during an integration period and establishing a V+ readout voltage during a readout period.

26. In an imager comprising an array of imager cells coupled to a multi-mode controller, a method for controlling the imager, the method comprising:

operating in a low-light operating mode by collecting electrons in a photoreceptor potential well and constrained by an integration potential well; and

after an integration period, activating a Snap mode comprising simultaneously transferring accumulated charge for a set of the imager cells to their sense nodes.

27. A method according to claim 26, further comprising selecting a plurality of imager cells as the set of the imager cells .

28. A method according to claim 27, wherein the set of imager cells comprises a rectangular sub-array of imager cells selected from the array of imager cells.

29. A method according to claim 26, wherein operating in a low-light operating mode comprises establishing a V- integration voltage during an integration period to setup the integration potential well and establishing a V+ readout voltage during a readout period.

30. A method according to claim 29 where establishing a V- integration voltage and establishing a V+ readout voltage comprises establishing a V- integration voltage and a V+ readout voltage on a photoreceptor readout gate.